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2 Tracking down software bugs using automatic anomaly detection

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8 Novel InP-channel HEMTs grown by organometallic vapor phase epitaxy

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9 Growth of high purity InP and fabrication of high sensitivity InP/GaInAs heterojunction phototransistors on silicon by OMVPE

Aina, L.; Mattingly, M.; Burgess, M.; O'Connor, J.M.; Shastry, S.K.; Hill, D.S.; Salerno, J.P.; Davis, A.;
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10 0.33- μ m gate-length millimeter-wave InP-channel HEMTs with high f_1 and f_{\max}

Aina, L.; Burgess, M.; Mattingly, M.; O'Connor, J.M.; Meerschaert, A.; Tong, M.; Ketterson, A.; Adesida, I.;
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11 High voltage DMOS power FETs on thin SOI substrates

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1 Cycle-accurate energy estimation in system level descriptions of embedded systems

Belen Abril Garcia, A.; Gobert, J.; Dombek, T.; Mehrez, H.; Petrot, F.;
Electronics, Circuits and Systems, 2002. 9th International Conference on , Volume: 2 , 15-18 Sept. 2002
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Wong, S.; Cotofana, S.; Vassiliadis, S.;
Parallel and Distributed Processing, 2001. Proceedings. Ninth Euromicro Workshop on , 7-9 Feb. 2001
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Burtscher, M.; Zorn, B.G.;
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[\[Abstract\]](#) [\[PDF Full-Text \(1116 KB\)\]](#) [IEEE CNF](#)**4 Cycle-accurate simulation of energy consumption in embedded systems**

Simunic, T.; Benini, L.; De Micheli, G.;
Design Automation Conference, 1999. Proceedings. 36th , 21-25 June 1999
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[\[Abstract\]](#) [\[PDF Full-Text \(600 KB\)\]](#) [IEEE CNF](#)**5 Exploring last n value prediction**

Burtscher, M.; Zorn, B.G.;
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Bechem, C.; Combs, J.; Utamaphethai, N.; Black, B.; Blanton, R.D.S.; Shen, J.P.;
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7 Performance analysis and validation of the picoJava processor*Hangal, S.; O'Connor, M.;*

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Application-Specific Systems, Architectures and Processors, 1997. Proceedings., IEEE International Conference on, 14-16 July 1997

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1 Exploring the cache design space for web servers*Iyer, R.;*

Parallel and Distributed Processing Symposium., Proceedings 15th International , 23-27 April 2001

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Software Engineering, IEEE Transactions on , Volume: 26 Issue: 11 , Nov. 2000

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[\[Abstract\]](#) [\[PDF Full-Text \(520 KB\)\]](#) **IEEE JNL****3 Performance analysis and validation of the picoJava processor***Hangal, S.; O'Connor, M.;*

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6 Advanced alterable pipeline timer (adapt): a tool to design a high performance PowerPC™ microprocessor

Burgess, B.G.; Plummer Litch, S.;

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7 Uninterpreted co-simulation for performance evaluation of Hw/Sw systems

Calvez, J.P.; Heller, D.; Pasquier, O.;

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8 Optimal on-chip cache hierarchy synthesis with scaling of technology

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9 Performance modeling of the interconnect structure of a three-dimensional integrated RISC processor/cache system

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10 Timing analysis for synthesis of hardware interface controllers using timed signal transition graphs

Escalante, M.A.; Dimopoulos, N.J.; Gyuroff, D.; Muller, H.;

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MacDonald, R.; Srinivasan, S.; Williams, R.; Aylor, J.;
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